

科目：電子學 適用：電機系三

編號：831

考生注意：

1. 依次序作答，只要標明題號，不必抄題。
2. 答案必須寫在答案卷上，否則不予計分。
3. 限用藍、黑色筆作答；試題須隨卷繳回。

本 試 題

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1. In Fig. 1 the diode has a voltage drop  $V_D = 0.8V$ .

(a) Use Thevenin's theorem to simplify the circuit and, [5%]

(b) hence calculate the diode current  $I_D$  [5%]

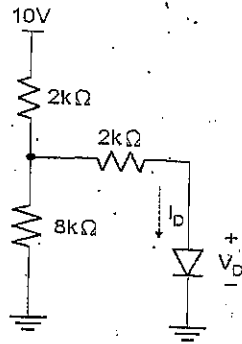


Fig. 1

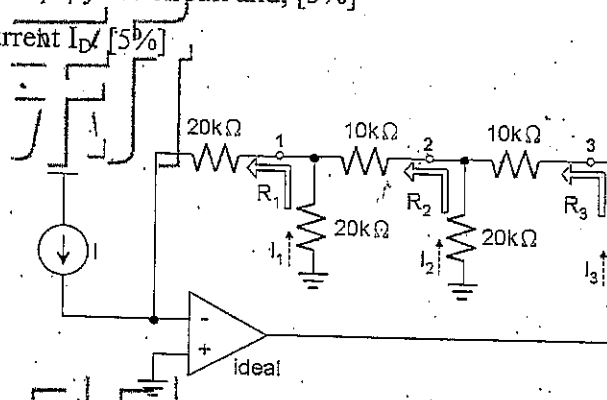


Fig. 2

2. The OP amplifier in Fig. 2 is ideal.

(a) What are the characteristics of an ideal OP amplifier? [5%]

(b) Find the resistances looking into node 1,  $R_1$ ; node 2,  $R_2$ ; and node 3,  $R_3$ . [5%]

(c) Find the current  $I_1$ ,  $I_2$ , and  $I_3$  in terms of the input current  $I$ . [5%]

3. In Fig. 3, assume  $V_{id} = V_2 - V_1$ , find the differential voltage gains of  $A_m$  and  $A_o$ , where  $A_m = V_m/V_{id}$ ,  $A_o = V_o/V_{id}$ . [20%]

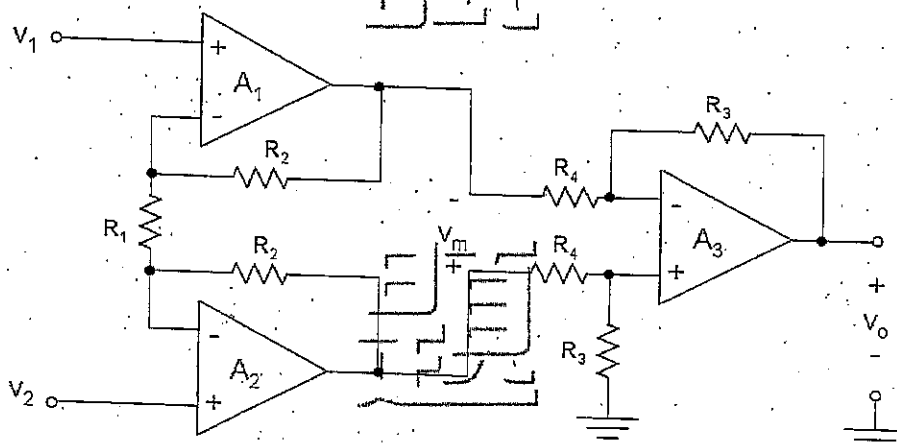


Fig. 3

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4. In Fig. 4, assume all of the transistors are operating in saturation. Derive  $I_{copy}$  for the following two circuits. [10%]

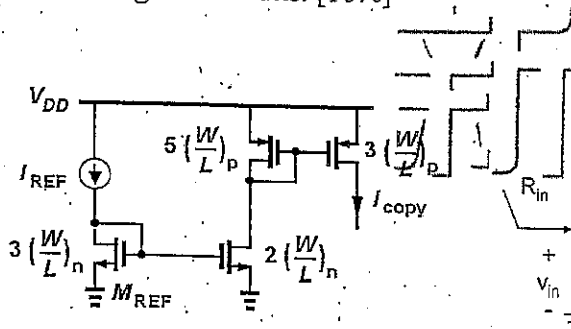


Fig. 4

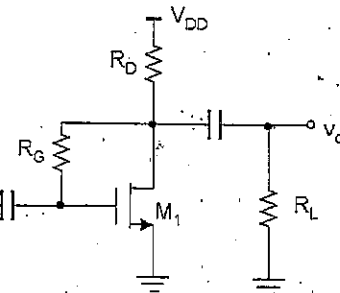


Fig. 5

5. In Fig. 5, assume the capacitors to be sufficiently large so as to act as short circuit at the signal frequencies of interest.  $V_{DD} = 7V$ ,  $R_G = 10M\Omega$ ,  $R_D = 5K\Omega$ ,  $R_L = 5K\Omega$ ,  $M_1$  has  $V_t = 1V$ ,  $k'_n(W/L) = 0.4 mA/V^2$ , and  $V_A = 40V$ . Find
- (a) the dc operating point, [5%]
  - (b) the small-signal equivalent circuit, [5%]
  - (c) the voltage gain  $A_v = v_o/v_{in}$ , [5%]
  - (d) and the input resistance  $R_{in}$ , [5%]

6. To design a CE stage of Fig. 6 for a voltage gain of 20, what is the minimum allowable supply voltage if  $Q_1$  must remain in the active mode? Assume  $V_A = \infty$  and  $V_{BE} = 0.8V$ . [10%]

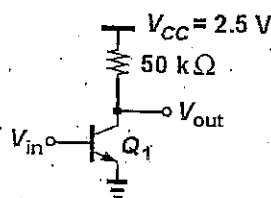


Fig. 6

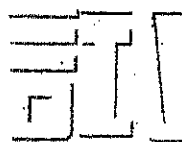


Fig. 7

7. For the circuit in Fig. 7, draw its voltage transfer characteristics, i.e. the plot of  $V_i$  vs.  $V_o$ . Assume  $V_{CC} = 5V$ ,  $R_B = 10k\Omega$ ,  $R_C = 1k\Omega$ ,  $\beta = 50$ , and  $V_{CEsat} = 0.2V$ . [10%]
8. Translate the following paragraph into Chinese. [5%]

"CMOS (complementary metal oxide semiconductor) technology is reliable, manufacturable, low power, low cost, and, perhaps most importantly, scalable. The fact that silicon integrated circuit technology is scalable was observed and described in 1965 by Intel founder Gordon Moore. His observations are now referred to as Moore's law and state that the number of transistors on a chip will double every 18 months."