

(本試題共 3 頁, 第 1 頁)

考生注意: 1. 依次序作答, 只要標明題號, 不必抄題。
2. 答案必須寫在答案卷上, 否則不予計分。
3. 試題隨卷繳回。

1. Fig. 1 shows an op amp connected in the non-inverting configuration. The op amp has an open-loop gain μ , a differential input resistance R_{id} , and an output resistance r_o . Please use the feedback method to analyze the circuit. Find expressions for A , β , the closed-loop gain V_o/V_s , and the input resistance R_{in} . (20 %)

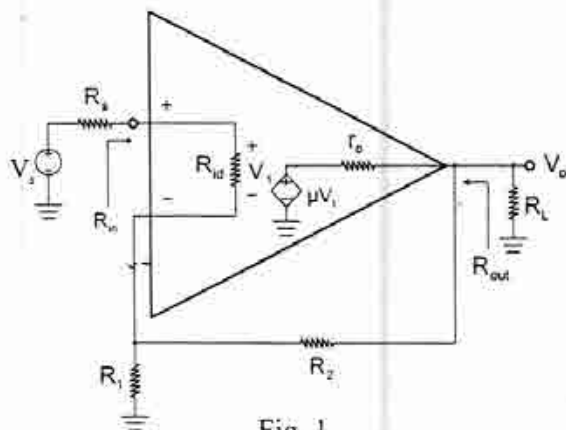


Fig. 1

2. Fig. 2 shows a commonly used configuration of LC-tuned oscillator known as the **Colpitts** oscillator. If the frequency of operation is low enough, then the transistor capacitances can be neglected. Please show that the frequency of

oscillation can be expressed as follows: $\omega_o = 1/\sqrt{L(\frac{C_1 C_2}{C_1 + C_2})}$. (15 %)

3. Fig. 3 shows a class B output stage circuit.

- (a) Please plot the transfer characteristic (i.e. v_o vs. v_i) (7 %)
(b) Please modify the circuit to reduce the crossover distortion. (8 %)

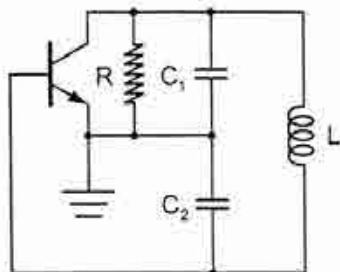


Fig. 2

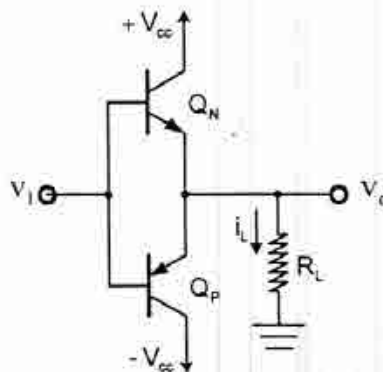


Fig. 3

(本試題共 3 頁, 第 2 頁)

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4. The following parameters are given for an NPN transistor with current polarities shown in Fig. 4:

I_{CO} : reverse saturation current for base-collector junction

I_{EO} : reverse saturation current for base-emitter junction

α_F : forward α

α_R : reverse α

V_T : thermal voltage

- (a) Please draw the **Ebers-Moll** model for the transistor. (6%)
 (b) Write down the Ebers-Moll expressions for I_E and I_C . (6%)
 (c) When the transistor is in normal mode of operation, please show that (assume $\alpha_R \ll 1$):

$$I_C = \alpha_F I_E + I_{CO}$$

$$I_C = \beta_F I_B + (\beta_F + 1) I_{CO} \quad (6\%)$$

where $\beta_F = \frac{\alpha_F}{1 - \alpha_F}$

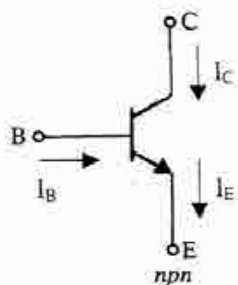


Fig. 4

5. (a) What are the main parameters in a BJT that would affect its bias stability? (3%)

- (b) The bias stability factor S_I is defined as $S_I = \frac{\partial I_C}{\partial I_{CO}} \equiv \frac{\Delta I_C}{\Delta I_{CO}}$ in a BJT. For the bias

circuit shown below (Fig. 5), please find the expression for S_I in terms of R_B , R_E and β_F and determine how the bias stability can be improved. (8%)

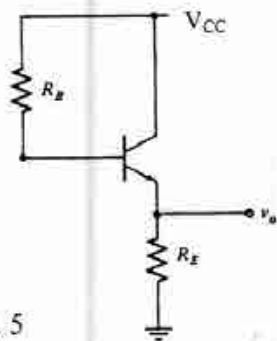


Fig. 5

(本試題共 3 頁, 第 3 頁)

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6. (a) Write down the expressions for the output resistance of the following two MOS current mirrors shown in Figs. 6(a) and 6(b). (8%)
(b) Compare with the current mirror in Fig. 6(b), what is the advantages and disadvantages of the MOS current mirror given in Fig. 6(c). (5%)

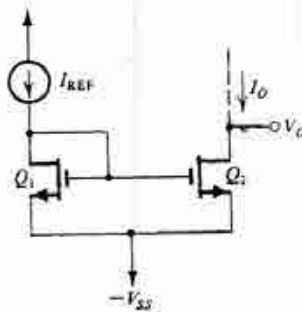


Fig. 6(a)

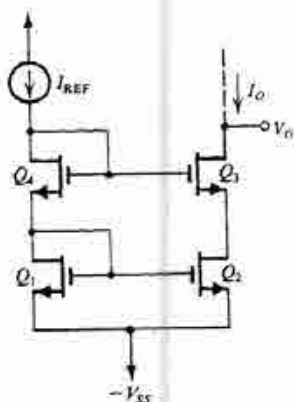


Fig. 6(b)

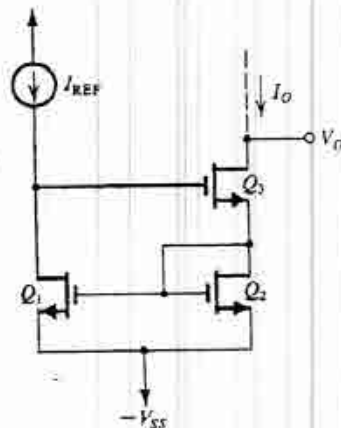


Fig. 6(c)

7. Consider a Miller integrator circuit shown in Fig. 7. If the input bias currents of the op amp are I_{B1} and I_{B2} for the inverting input and non-inverting input, respectively. Let the average input bias current $I_B = \frac{1}{2}(I_{B1} + I_{B2})$, and the input offset current $I_{OS} = |I_{B1} - I_{B2}|$. Assume the capacitor voltage is zero at $t = 0$, please find the output voltage caused by the input bias currents in terms of I_B and I_{OS} if the integrator input terminal is connected to the ground. (8%)

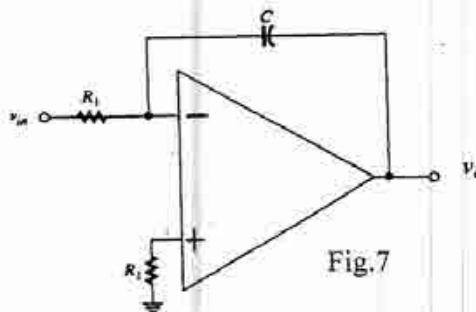


Fig. 7