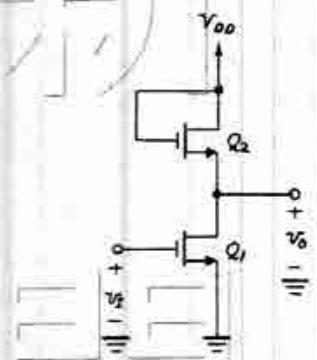
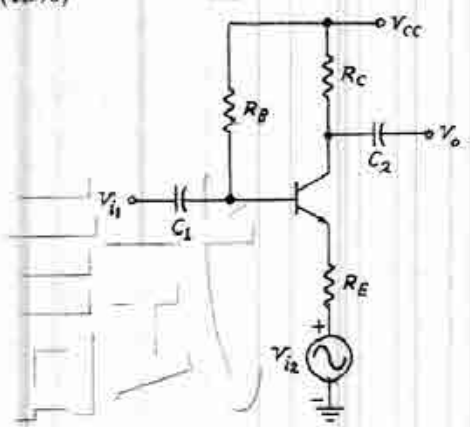
考生注意: 1. 依次序作答，只要標明題號，不必抄題。
2. 答案必須寫在答案卷上，否則不予計分，並限以藍黑色筆作答。
3. 試題隨卷繳回。(餘請詳閱試場規則)

1. **The circuit shown below is an NMOS amplifier with enhancement load. Assume that the channel-length-modulation effect and body effect can be neglected, please show that the voltage gain of the amplifier can be expressed as:**

$$A_v = -\sqrt{\frac{(W/L)_1}{(W/L)_2}}$$ **(15%)**



2. **If the BJT in the circuit shown below has been biased in its forward active region, please find the expression for the output voltage V_o in terms of the two input signals V_{i1} and V_{i2}. (15%)**



3. **(a) Please plot the minority carrier distribution in a PN junction under forward bias and reverse bias. (10%)**
   (b) Explain why there exists a minority carrier storage time in a PN junction that is driven from the forward-state to the reverse state. (10%)

4. **(a) Calculate the dc offset voltage (V_{OS}) of the MOS differential pair shown below caused by mismatch in threshold voltage V_t. (16%)**
   (b) Give the other two factors that contribute to the dc offset voltage of the

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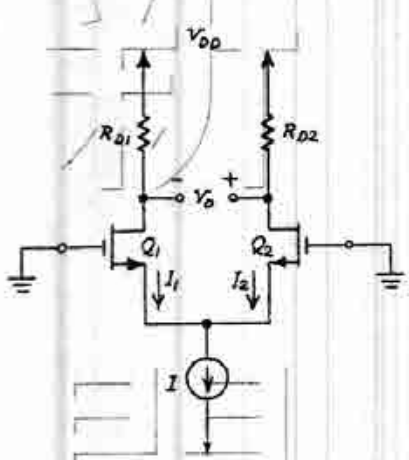
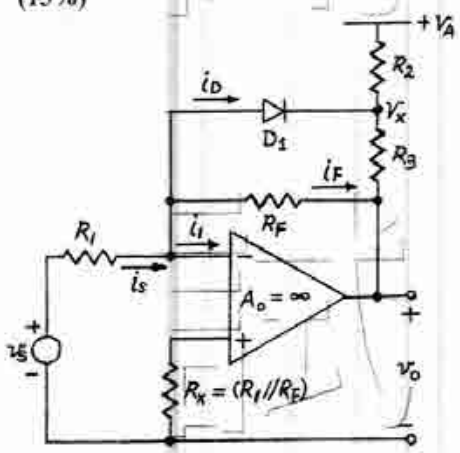
MOS differential pair. (4%)



5. For the circuit shown below, please determine its voltage transfer characteristic. (15%)



6. (a) The open-loop gain of an amplifier is given by $A(s) = \frac{1}{s^2 + 3}$. Determine the close-loop step response of the amplifier. Is the amplifier stable or unstable? (9%) (Assuming $\beta(s) = 1$)

(b) Define the phase margin and gain margin of a feedback amplifier. (6%)