科目：**413** 計算機結構

系組：資工系

考生注意：1. 依次序作答，只要標明題號，不必抄題。
2. 答案必須寫在答案卷上，否則不予計分。
3. 試題隨卷繳回。

The following problems may be answered in Chinese or English. You need to give all details in order to receive credit (point).

1. **(20 points)** Design a parallel adder to add eight 3-bit numbers using the Wallace trees technique.

2. **(20 points)** When a branch or interrupt occurs, the pipeline will lose many cycles to handle the out-of-order operations. Describe two techniques to overcome this difficulty

3. **(10 points)** Figure P3 shows a small write update on RAID 3 versus RAID 4/RAID 5. This figure assumes we have four blocks of data and one block of parity. Describe the small write operations on RAID 3 and RAID 4/RAID 5. How many disk drives are involved in each case?

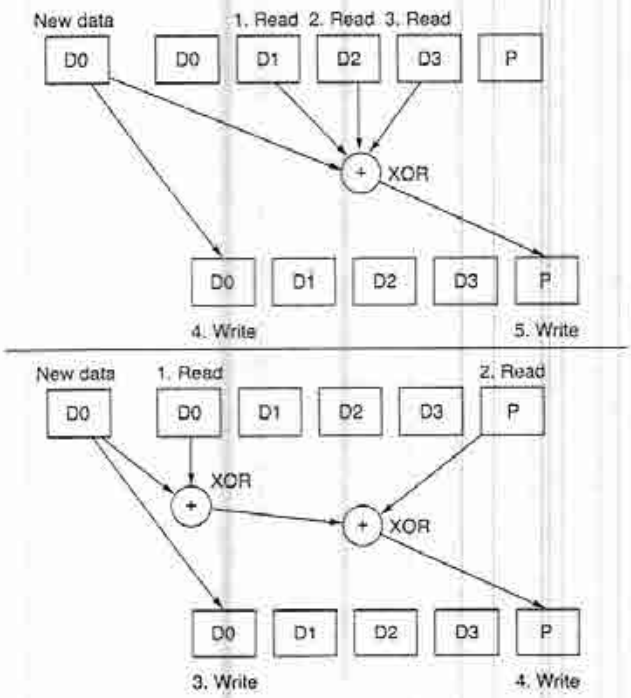

Figure P3. Small write update on RAID 3 (top) versus RAID 4/Raid 5 (bottom).

4. **(20 points)** Suppose we have made the following measurements:

   Frequency of FP operations (other than FPSQR) = 25%
   Frequency of FPSQR = 2%
   Average CPI of FP operations = 4.0
   Average CPI of other instructions = 1.33
   CPI of FPSQR = 20

   Assume that the two design alternatives (with the same clock cycle) are to decrease the CPI of FPSQR to 2 or to decrease the average CPI of all FP operations to 2.5. Using the CPU performance equation, compare these two design alternatives by comparing the speedups.

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5. **(30 points)** The following loop computes Y[i] = a×X[i]+Y[i], the key step in a Gaussian elimination. Assume the pipeline latencies from Figure P5.1 and a 1-cycle delayed branch.

```
loop:  L.D     F0, 0(R1)     ;load X[i]
       MUL.D   F0, F0, F2    ;multiply a×X[i]
       L.D     F4, 0(R2)     ;load Y[i]
       ADD.D   F0, F0, F4    ;add a×X[i]+Y[i]
       S.D     0(R2), F0     ;store Y[i]
       DSUBUI  R1, R1, #8    ;decrement X index
       DSUBUI  R2, R2, #8    ;decrement Y index
       BNEZ    R1, loop      ;loop if not done
```

a. Assume a single-issue pipeline. Unroll the loop as many times as necessary to schedule it without any delays. Collapsing the loop overhead instructions. Show the schedule. What is the execution time per element?

b. Assume a dual-issue processor as in Figure P5.2. Unroll the loop as many times as necessary to schedule it without any delays. Collapsing the loop overhead instructions. Show the schedule. What is the execution time per element? How many instruction issue slots are unused?

Instruction producing result	Instruction using result	Latency in clock cycle
FP ALU op	Another FP ALU op	3
FP ALU op	Store double	2
Load double	FP ALU op	1
Load double	Store double	0

Figure P5.1 Latency of FP operations used in this problem.

	Integer instruction		FP instruction		Clock cycle
Loop:	L.D	F0,0(R1)			1
	L.D	F6,–8(R1)			2
	L.D	F10,–16(R1)	ADD.D	F4,F0,F2	3
	L.D	F14,–24(R1)	ADD.D	F8,F6,F2	4
	L.D	F18,–32(R1)	ADD.D	F12,F10,F2	5
	S.D	0(R1),F4	ADD.D	F16,F14,F2	6
	S.D	–8(R1),F8	ADD.D	F20,F18,F2	7
	S.D	–16(R1),F12			8
	DADDUI	R1,R1,#–40			9
	S.D	16(R1),F16			10
	BNE	R1,R2,Loop			11
	S.D	8(R1),F20			12

Figure P5.2 The unrolled and scheduled code as it would look on a superscalar MIPS.