1. (**10 points**) If memory access time is 200 ns and page fault rate is 0.0000025, what is the maximum page fault service time such that the effective memory access time does not exceed 210 ns?
2. (**10 points**) Assume that both the logical and physical address are 16-bits wide, the page size is 1K (1024) bytes, and one-level paging is used.
   A. (5 pts) How many entries are there in the page table?
   B. (5 pts) If the logical address is still 16-bits wide, but the physical address is extended to 20 bits wide. In order to do the 16 to 20 mapping, some modification to the original page table is needed. What's it?
3. (**10 points**) For the following code, explain how you figure out the number of processes generated (including the initial one). Assume all invocations of fork() are successful.

```
k = 0;
while( k < 2 )
    if( fork() == 0 )
        k += 1;
    else
        k += 2;
```

4. (**20 points**) Answer Yes or No for following questions. Each correct answer gets 5 points.
   A. The instruction to read the clock should be privileged.
   B. The instruction to issue a trap is not privileged.
   C. The LRU page replacement algorithm does always perform well.
   D. Context-switch does affect the performance of cache.

5. (**10 points**) True or false
   A. (2 pts) Moore's law indicates that, the power consumption of a chip doubles every year.
   B. (2 pts) Most of our personal computers and smartphone devices utilize Von-Neumann architecture.
   C. (2 pts) For single instruction, its execution is longer when the pipeline stage number is larger.
   D. (2 pts) Pipeline hazards surely cause pipeline stalls.
   E. (2 pts) Adding duplicate resources must be able to reduce latency of a job that cannot be parallelized.

6. (**16 points**)Performance and energy evaluations:
   A company has developed a computer system, and the instruction set of the computer has three types, A, B and C. When running the computer's target workload, the CPI (Clock Cycle per Instruction) and IC (Instruction Count) results are shown in Table 1.

Under this design, the computer's average power consumption is 20W. The engineers in the company developed two kinds of improvements for the computer, called Alpha and Beta. Improvement Alpha lowers the IC of C type instruction from 0.5M to 0.1M, and the CPI of C type instruction from 3 to 1.5. However, Alpha increases the average power consumption to 30W. Improvement Beta, on the other hand, lowers the CPI of A type instruction from 2 to 1 while the overall power consumption is increased to 21W. Please answer the following questions. Please show me your deduction process to get the full scores.

A. (8 pts) In terms of performance, which improvement do you recommend?
B. (8 pts) In terms of energy consumption, which improvement do you recommend?

Table 1 CPI and IC of the target workload running on the computer

Instruction Type	A	B	C
CPI	2	1	3
IC	1M	0.5M	0.5M

- M: Million

7. (**12 points**) Pipeline

Given the following assembly code, answer the questions.

```
lw      R1, 0(R2)
add     R3, R1, R4
add     R5, R3, R6
add     R7, R8, R9
```

A. (3 pts) Explain data hazard.
B. (3 pts) Identify the data hazard in the code.
C. (3 pts) Explain instruction scheduling
D. (3 pts) Can you remove pipeline stalls caused by data hazard in the code? If yes, how do you achieve this?

8. (**12 points**) Cache

Assume we have a direct mapped cache of capacity 2MB, and block size of 256B.

A. (3 pts) In a memory hierarchy, where is cache usually located?
B. (3 pts) How many cache blocks in the target cache?
C. (3 pts) Show me the binary form of memory address 0x 1A88 99F2
D. (3 pts) Which set does the above address mapped to?