

科目：計算機概論

適用：電機系三

編號：745

考生注意：

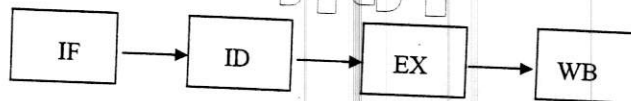
1. 依次序作答，只要標明題號，不必抄題。
2. 答案必須寫在答案卷上，否則不予計分。
3. 限用藍、黑色筆作答；試題須隨卷繳回。

本 試 題
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- 1 • (1) What is "Predict Not Taken" in CPU pipeline design? (15%)
(2) Please describe the advantage and disadvantage of "Predict Not Taken". (15%)

- 2 • Please briefly describe the function of the four-pipeline architecture as follows:

- (1) Instruction Fetch (IF) (8%)
- (2) Instruction Decode (ID) (7%)
- (3) Execution (EX) (8%)
- (4) Write Back (WB) (7%)



- 3 • What is **Data Hazard** in CPU pipeline design? (10%)
What is **Control Hazard** in CPU pipeline design? (10%)

- 4 • The format of "24-bits Floating point" (IEEE 754) is shown as follows.

1	8	15
S	Exp	Mantissa

- (1) What is the biggest positive value? (5%)
- (2) What is the smallest negative value? (5%)
- (3) What is the value of "0 10000000 0100000000000000"? (5%)
- (4) What is the value of "0 10000001 1000000000000000"? (5%)

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