You may answer the following questions in Chinese or English.

1. (10 points)
What are the possible outputs of the following program?
(Assume the new process is created successfully.)

```
#include <sys/types.h>
#include <stdio.h>
#include <unistd.h>
int main()
{
   int value = 2016;
   if(fork() <= 0) {
     value += 8;
     printf("The value is %d\n", value);
   } else {
     printf("The value is %d\n", value);
     wait(NULL);
   }
   printf("Over with %d\n", value);
}
```

2. (20 points)
   (a) (10 points) Assume that virtual address is 16-bits wide and physical address is 24-bits wide. The page size is 4K bytes. If the mapping is done by one level paging, how many entries are there in the page table?
   (b) (10 points) The memory access time is 10 ns. But if page fault occurs, the time becomes 10 ms. If the effective access time is not over 11 ns, what is the maximum page fault rate?

3. (20 points)
Please give a short description and yes/no for each question. (5 points for each)
   (a) The instruction to issue a trap is privileged.
   (b) The instruction to read the clock is privileged.
   (c) A non-preemptive kernel, running on an uni-processor system, can enforce data integrity through disable/enable interrupt.
   (d) The LRU page replacement algorithm always performs well.

4. True or false (15 points)
   a. (3 pts) For a CPU with pipeline, the number of pipeline stage has to be fixed at five.
   b. (3 pts) A "parallel computer" indicates a computer with multiple processing elements that can process several independent tasks in parallel.
   c. (3 pts) Processors that execute different instruction sets can have exactly the same micro-architecture.
   d. (3 pts) For a CPU that utilizes pipeline, more than one instruction may be in the pipeline at the same time.
   e. (3 pts) A program without any temporal and spatial locality can still have performance gain from utilizing memory hierarchy.

5. (6 points) Compared to a multi-cycle datapath, how does pipeline help improve performance?

6. (4 points) Explain von Neuman architecture.

7. (10 points) Explain the reason that the design of memory hierarchy is helpful to performance.

8. (15 points) CPU time and performance
   a. (3 pts)The CPU time of a program can be calculated by the CPI (clock cycle per instruction) and IC (instruction count) of running the program on the target CPU, and the CT (clock cycle time) of the target CPU. Please list the formula for estimating CPU time, where the CPI, IC and CT are used for calculating the CPU time.
   b. (8 pts)Given a program P and two CPUs, $CPU_A$ and $CPU_B$, the CPIs and ICs of executing P on $CPU_A$ and $CPU_B$, and the cycle times of $CPU_A$ and $CPU_B$, are listed in the following table. Compare the performance of $CPU_A$ and $CPU_B$ in terms of MIPS (Millions Instructions Per Seconds) and CPU time.

| | Average CPI | IC | Clock Cycle Time |
|---|---|---|---|
| $CPU_A$ | 2 | 100 | 100ns |
| $CPU_B$ | 2.5 | 75 | 110ns |

   c. (4 pts)Given a target system with program P running on CPU A, assume we have a performance improvement technique that would make 30% of program P with 100 times speedup while the performance of the other 70% stays the same, how much overall speedup would the improvement technique get?